PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)* see form PCT/ISA/210 (second sheet)	
Applicant's or agent's file reference see form PCT/ISA/220	**FOR FURTHER ACTION** See paragraph 2 below
International application No. PCT/GB2004/002999	International filing date *(day/month/year)* 09.07.2004
Priority date *(day/month/year)* 12.07.2003	
International Patent Classification (IPC) or both national classification and IPC H01L51/40, H01L21/28	
Applicant HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.	

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☒ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Pusch, C Telephone No. +49 89 2399-7023

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/GB2004/002999

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing:

   ☐ contained in the international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non obvious), or to be industrially applicable have not been examined in respect of:

☐ the entire international application,

☒ claims Nos. 56-58

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination *(specify)*:

☒ the description, claims or drawings *(indicate particular elements below)* or said claims Nos. 56-58 are so unclear that no meaningful opinion could be formed *(specify)*:

see separate sheet

☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

☐ no international search report has been established for the whole application or for said claims Nos.

☐ the nucleotide and/or amino acid sequence listing does not comply with the standard provided for in Annex C of the Administrative Instructions in that:

the written form	☐	has not been furnished
	☐	does not comply with the standard
the computer readable form	☐	has not been furnished
	☐	does not comply with the standard

☐ the tables related to the nucleotide and/or amino acid sequence listing, if in computer readable form only, do not comply with the technical requirements provided for in Annex C-*bis* of the Administrative Instructions.

☒ See separate sheet for further details

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has:

   ☐ paid additional fees.

   ☒ paid additional fees under protest.

   ☐ not paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☒ all parts.

   ☐ the parts relating to claims Nos.

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	25-55
	No:	Claims	1-16,18-24
Inventive step (IS)	Yes:	Claims	25-55
	No:	Claims	1-24
Industrial applicability (IA)	Yes:	Claims	1-17,25-58
	No:	Claims	

2. Citations and explanations

   see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY (SEPARATE SHEET)

International application No.
PCT/GB2004/002999

Re Item III.

It is attempted to define device claim 56 by reference to the 7 method claims 49 - 55. The scope of protection for this claim and for "omnibus" claims 57 and 58 as such is not clear, contrary to Rule 6.2(a) PCT.
Claims 56 - 58 are not discussed in this written opinion.

Re Item IV.

An electrode formed by electrodeposition is not considered to be always and unambiguously distinguishable from one formed by other prior art methods. The feature in claims 1 and 9 of electrodes being formed by electrodeposition is not discernable in the final semiconductor device, and is therefore disregarded in assessing the patentability of these claims. The device features directly discernable in the semiconductor device of claim 1 and 9 are however known from D1 or D6 (see items 2.1 and 2.3 below). The requisite unity of invention (Rule 13.1 PCT) therefore no longer exists inasmuch as a technical relationship involving one or more of the same or corresponding special technical features in the sense of Rule 13.2 PCT does not exist between the subject-matter of the following groups of dependent claims:

Claims 10 - 17: bottom-gate FET with source and drain in one plane, gate in another
claims 18 - 23: FET with source-gate-drain in one plane

Re Item V.

1.0 The following documents are referred to in this communication:

D1: EP-A-1 263 062, 4 December 2002
D2: CN1398004, 19 February 2003 & EP-A-1 394 873, 3 March 2004
D3: US 6 555 411, 29 April 2003
D4: US2003/0108727, 12 June 2003
D5: US 3 990 926, 9 November 1976
D6: EP-A-1 085 578, 21 March 2001
D7: US2002/0008464, 24 January 2002

D8: US2002/0093017, 18 July 2002
D9: WO 02/065557, 22 August 2002
CN1398004 and EP-A-1 394 873 belong to the same patent family. It is therefore assumed that both documents contain the same degree of disclosure. It is cited from the European application as the translation of the Chinese document only. The Chinese document was published before the priority date of the present application and therefore forms part of the prior art. The European application was published after the priority date and before the filing date of the present application.

Device claims 1 - 17, and 24

2.0 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1 - 16 and 24 is not new in the sense of Article 33(2) PCT.

2.1 The document D1 discloses (the references in parentheses applying to this document):

A semiconductor device (abstract) comprising:
a first electrode component ("106" in fig. 1);
a second electrode component ("107" in fig. 1);
a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component;
a second layer ("105" and "106" in fig. 1) having a portion comprising deposited semiconductor material ("106" in fig. 1) contacting the first and the second electrode components; and
a third layer comprising a substrate ("101" in fig. 1),
wherein the first second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer

The subject-matter of claim 1 lacks novelty.

2.2 The subject-matter of claims 2, 3 (col. 5, l. 19-20), the insulated film fixes the device to the silicon substrate), 4, 5, 6 (paragraph [0022]), 7, 9, 10 ("102" in fig. 1), 11, 12

(col. 5, l. 19-20), 13, 15, 16 ("105" in fig. 1), and 24 (abstract, "matrix type organic semiconductor device" on an insulated surface = substrate) are also known from D1. Their subject-matter lacks novelty.

2.3 D6, too, describes the semiconductor device of claim 1 (example 2 and fig. 6; third layer: glass substrate "601", second layer fig. 6© without glass substrate "601", first layer "608" and "608'" and electrodeposited electrodes (p. 15, l. 15 or 32)), rendering the subject-matter of device claim 1 not new.

2.4 The features of claims 2, 3, 4, 6, 7 (paragraph [0091]), 9 (FET), 10 (fig. 7(e)), 11 (as the gate controls the current in the semiconductor it must necessarily be somehow aligned with the semiconductor), 14, 15 (fig. 6(f) or 7(e) show substantially planar surfaces) are known from D6 and therefore their subject-matter is not new.

2.5 The document D2 discloses the features of claim 1 (paragraphs [0014] or [0020]/[0021] or [0031] and fig. 2, first layer: "5", second layer: "4", third layer: "1". The teaching of D2 is also novelty destroying for the subject-matter of claims 2, 4, 5, 8 (first line of paragraph [0021] or [0031]), 10, 11, 14 and 15 (fig. 2).

3.0 Should the feature of electrodes being formed by electrodeposition be discernable in the final device, then it is not inventive. It is known from D3 (abstract) or D6 (p. 15, l. 15 and l. 31) to form electrodes of a semiconductor device by electrodeposition. The skilled person will form the electrodes of the device of D1 or D2 by this method whenever circumstance makes it desirable.

3.1 Photopatternable gate dielectrics for organic FETs are known (see e.g. D9, p. 6, l. 10 - p. 7, l. 7) and can be structured without the need for a further photoresist. This advantage is not linked to a specif structure of a device. The inclusion of a paternable gate dielectric into any of the devices of D1, D2 or D6 is not inventive.

Device claims 18 - 23

4.0 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 18 - 23 is not new in the sense of Article 33(2) PCT.

4.1 The subject-matter of claims 18 (fig. 5(f)), 19, 20, 21, 22, 23 is known from D6 and therefore lacks novelty. Including the feature of an organic semiconductor in any of the claims 1, 9 or 18 would not render their subject-matter inventive over the teaching of D6, because organic semiconductor devices are known. As organic semiconductor materials can easily be deposited by liquid coating methods, it is obvious to the skilled person to apply an organic semiconductor in a device of D6.

4.2 The semiconductor device of claim 1 and the FET of claim 9 are known from D7 (paragraph [0034] and fig. 1). The geometry of the FET of claim 18 is also disclosed in D7, and consequently, the subject-matter of claim 18 lacks novelty.
As the features of claims 19 - 21, and 23 are described in D7, their subject-matter is not novel.
The insertion of a gate dielectric is common practice for field effect transistors and therefore the subject-matter of claim 22 is not inventive.

4.3 The semiconductor device of claim 1 and the FET of claim 9 are described in D8 (fig. 1(e) and paragraph [0006]). The geometric structure of claim 18 is also known from D8 (first layer "106", second layer "104", third layer "101") as are the features of claims 19 - 23.

Method claims 25 - 55

5.0 The subject-matter of method claims 25 and 49 is neither known from nor rendered obvious by the available prior art and thus considered new and inventive.

It is known from D3 (abstract) or D6 (p. 15, l. 15 or 32) to plate electrodes of a TFT. D4 describes transfer sheets suitable for the formation of electrode patterns, however, the electrode pattern is transferred unstructured and subsequently patterned without a photoresist (paragraphs [0182] - [0185])
A copper layer which has been formed by electroplating is transferred from a

temporary base to a final insulating base and then structured by etching in D5 (col. 5, l. 27 - 41 and 55 - 57). The thickness of the structured copper layer is increased by electroplating.

5.1 The subject-matter of dependent method claims 26 - 48 being dependent on claim 25 and of dependent method claims 50 - 55 being dependent on claim 49 is also new and inventive.

Re Item VIII.

6.0 The application does not meet the requirements of Article 6 PCT, because claims 1, 2, 3, 6, 9, 11, 13, 14, 15, 25, 28, 33, 49, 51, and 55 - 58 are not clear.

6.1 A known device cannot be rendered new or inventive by the method of its manufacture, even if this method is new and inventive. A device must be described by device features directly discernable in the final device which render the device as such new and inventive.
The feature of electrodeposited electrodes in claims 1 and 9 therefore lacks clarity as does the feature of the deposited semiconductor material in claim 6 "comprising indications that it was deposited from liquid".

6.2 Although method claims 25 and 49 have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and in respect of the terminology used for the features of that subject-matter. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of Article 6 PCT.

6.3 The term "substantially" used in claims 2, 13, 15, 28, 33, 51, and 55 is vague and unclear and leaves the reader in doubt as to the meaning of the technical features to which it refers, thereby rendering the definition of the subject-matter of said claims unclear.

6.4 The functional feature " the third layer fixes the substrate to the semiconductor device" in claim 3 is not clear. It is understood as a third layer between semiconductor and substrate.

6.5 As the no specific alignment of gate and semiconductor layer is mentioned in claim 11, the claim is not clear. Gate and semiconductor are necessarily somehow aligned in a thin film transistor.

6.6 Claim 14 cannot depend on claims 10 and 11 because a dielectric is first mentioned in claim 12 only.

6.7 see item III above for claims 56 - 58.